Table of Contents

[AOI21 2](#_Toc437810026)

[AOI22 6](#_Toc437810027)

[BUF 11](#_Toc437810028)

[DFF 19](#_Toc437810029)

[DFFNEGCLK 20](#_Toc437810030)

[DFFQ 21](#_Toc437810031)

[DFFQB 22](#_Toc437810032)

[INV 23](#_Toc437810033)

[MUXINV 30](#_Toc437810034)

[NAND 35](#_Toc437810035)

[NOR 40](#_Toc437810036)

[OAI21 46](#_Toc437810037)

[OAI22 50](#_Toc437810038)

[TIEHI 51](#_Toc437810039)

[TIELO 54](#_Toc437810040)

[TRINV 57](#_Toc437810041)

[XOR 61](#_Toc437810042)

# AOI21

**Cell Description:**This is a standard 3 input AND OR INVERT (AOI) cell. This cells functionality is described by the following Boolean equation:

**Truth Table:**

|  |  |  |  |
| --- | --- | --- | --- |
| **A** | **B** | **C** | **Y** |
| 0 | 0 | 0 | 1 |
| 0 | 0 | 1 | 0 |
| 0 | 1 | 0 | 1 |
| 0 | 1 | 1 | 0 |
| 1 | 0 | 0 | 1 |
| 1 | 0 | 1 | 0 |
| 1 | 1 | 0 | 0 |
| 1 | 1 | 1 | 0 |

**Behavioral Verilog:**//Verilog HDL for "Lib6710\_06", "AOI21X1" "behavioral"

module AOI21X1( Y, A, B, C );

input A;

input C;

output Y;

input B;

assign Y = ~((A&B) | C);

specify

(A => Y) = (1.0, 1.0);

(B => Y) = (1.0, 1.0);

(C => Y) = (1.0, 1.0);

endspecify

endmodule

**Cell Size:**

|  |  |  |
| --- | --- | --- |
| **Drive Strength** | **Height (μM)** | **Width (μM)** |
| AOI21X1 | 27.0 | 9.6 |

**Performance:**

**Propagation Delay (Rising Outputs):**

|  |  |  |
| --- | --- | --- |
| **Drive Strength** | **Min. (nS)** | **Max. (nS)** |
| AOI21X1 | 0.249604 | 3.820011 |

**Propagation Delay (Falling Outputs):**

|  |  |  |
| --- | --- | --- |
| **Drive Strength** | **Min. (nS)** | **Max. (nS)** |
| AOI21X1 | 0.367765 | 5.978167 |

**Output Fall Time:**

|  |  |  |
| --- | --- | --- |
| **Drive Strength** | **Min. (nS)** | **Max. (nS)** |
| AOI21X1 | 0.287229 | 4.7676 |

**Output Rise Time:**

|  |  |  |
| --- | --- | --- |
| **Drive Strength** | **Min. (nS)** | **Max. (nS)** |
| AOI21X1 | 0.207889 | 3.20355 |

**Logic Symbol:**

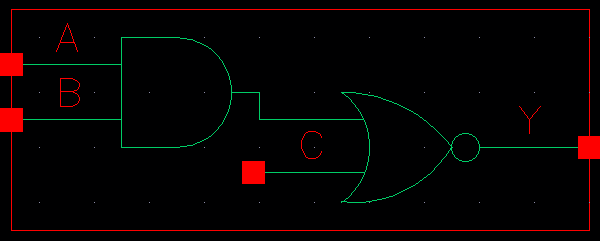
****

Figure 1: Symbol View for the AOI21 cell.

**CMOS Schematic:**The following figure displays the CMOS schematics for the AOI21 cell

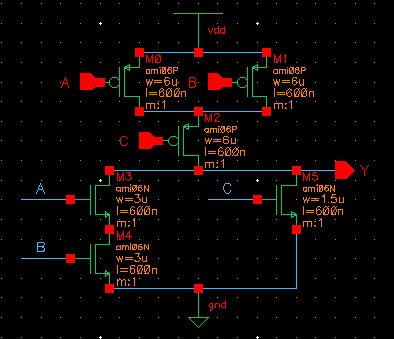
****

Figure 2: CMOS Schematic for the AOI21X1 cell.

**CMOS Layout:**

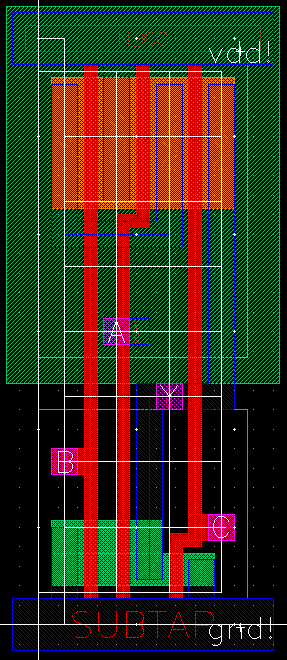
****

Figure 3: CMOS layout for the AOI21X1 cell.

# AOI22

**Cell Description:**This is a standard 4 input AND OR INVERT (AOI) cell. This cells functionality is described by the following Boolean equation:

**Truth Table:**

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| **A** | **B** | **C** | **D** | **Y** |
| 0 | 0 | 0 | 0 | 1 |
| 0 | 0 | 0 | 1 | 1 |
| 0 | 0 | 1 | 0 | 1 |
| 0 | 0 | 1 | 1 | 0 |
| 0 | 1 | 0 | 0 | 1 |
| 0 | 1 | 0 | 1 | 1 |
| 0 | 1 | 1 | 0 | 1 |
| 0 | 1 | 1 | 1 | 0 |
| 1 | 0 | 0 | 0 | 1 |
| 1 | 0 | 0 | 1 | 1 |
| 1 | 0 | 1 | 0 | 1 |
| 1 | 0 | 1 | 1 | 0 |
| 1 | 1 | 0 | 0 | 0 |
| 1 | 1 | 0 | 1 | 0 |
| 1 | 1 | 1 | 0 | 0 |
| 1 | 1 | 1 | 1 | 0 |

**Behavioral Verilog:**

//Verilog HDL for "Lib6710\_06", "AOI22x1" "behavioral"

module AOI22X1( Y, A, B, C, D );

input A;

input B;

output Y;

input C;

input D;

assign Y = ~((A&B) | (C&D));

specify

(A => Y) = (1.0, 1.0);

(B => Y) = (1.0, 1.0);

(C => Y) = (1.0, 1.0);

(D => Y) = (1.0, 1.0);

endspecify

endmodule

**Cell Size:**

|  |  |  |
| --- | --- | --- |
| **Drive Strength** | **Height (μM)** | **Width (μM)** |
| AOI22X1 | 27.0 | 12.0 |

**Performance:**

**Propagation Delay (Rising Outputs):**

|  |  |  |
| --- | --- | --- |
| **Drive Strength** | **Min. (nS)** | **Max. (nS)** |
| AOI22X1 | 0.257172 | 3.554636 |

**Propagation Delay (Falling Outputs):**

|  |  |  |
| --- | --- | --- |
| **Drive Strength** | **Min. (nS)** | **Max. (nS)** |
| AOI22X1 | 0.280125 | 3.91496 |

**Output Fall Time:**

|  |  |  |
| --- | --- | --- |
| **Drive Strength** | **Min. (nS)** | **Max. (nS)** |
| AOI22X1 | 0.209476 | 3.092532 |

**Output Rise Time:**

|  |  |  |
| --- | --- | --- |
| **Drive Strength** | **Min. (nS)** | **Max. (nS)** |
| AOI22X1 | 0.213544 | 3.512859 |

**Logic Symbol:**

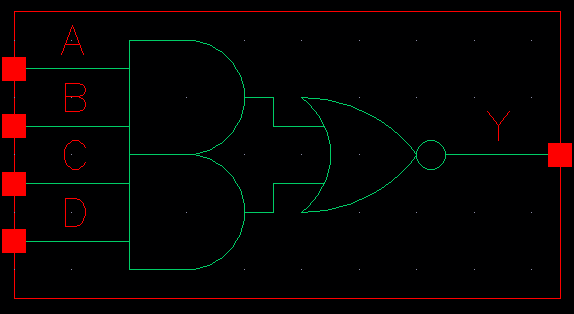
****

Figure 1: Symbol View for the AOI22 cell.

**CMOS Schematic:**

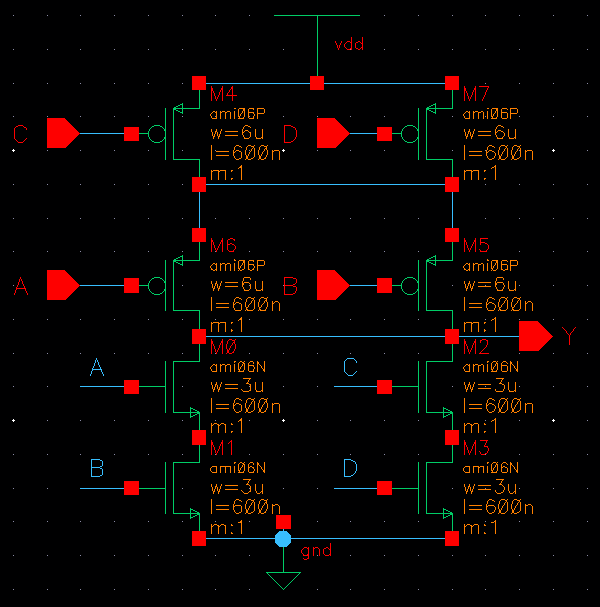
****

Figure 2: CMOS Schematic for the AOI22X1 cell.

**CMOS Layout:**

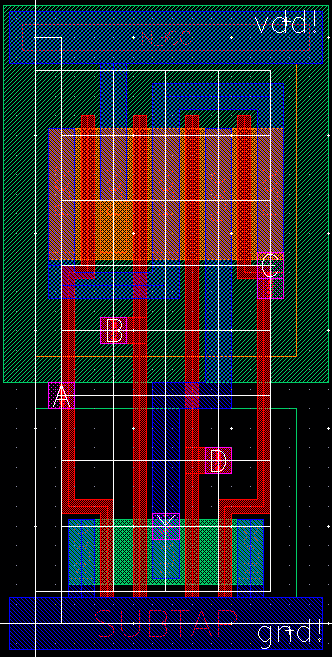
****

Figure 3: CMOS layout for the AOI22X1 cell.

# BUF

**Cell Description:**

This is a standard buffer cell with the following Boolean equation.

Each buffer is constructed by two inverters in series. To compensate for rise and fall times the input inverter is scaled appropriately by required drive strength of the output. In this cell library the both the BUFX2 and BUFX4 are driven by an inverter with a drive strength of 1, and the BUFX8 is driven by an invert with a drive strength of 2.

**Truth Table:**

|  |  |
| --- | --- |
| A | Y |
| 0 | 0 |
| 1 | 1 |

**Behavioral Verilog:**The behavioral Verilog for the inverter is independent of its drive strength. Replace the N in the module name with the respective drive strength (i.e. 1, 2, and 4).

//Verilog HDL for "Lib6710\_06", "BUFX2" "behavioral"

module BUFX2 ( Y, A );

input A;

output Y;

buf \_i0(Y,A);

specify

(A => Y) = (1.0, 1.0);

endspecify

endmodule

**Cell Size:**

|  |  |  |
| --- | --- | --- |
| **Drive Strength** | **Height (μM)** | **Width (μM)** |
| BUFX2 | 27.0 | 7.2 |
| BUFX4 | 27.0 | 7.2 |
| BUFX8 | 27.0 | 9.6 |

**Performance:**

**Propagation Delay (Rising Outputs):**

|  |  |  |
| --- | --- | --- |
| **Drive Strength** | **Min. (nS)** | **Max. (nS)** |
| BUFX2 | 0.460967 | 4.271176 |
| BUFX4 | 0.550102 | 4.247614 |
| BUFX8 | 0.453907 | 4.082325 |

**Propagation Delay (Falling Outputs):**

|  |  |  |
| --- | --- | --- |
| **Drive Strength** | **Min. (nS)** | **Max. (nS)** |
| BUFX2 | 0.428696 | 4.678109 |
| BUFX4 | 0.468653 | 4.338193 |
| BUFX8 | 0.433059 | 4.346652 |

**Output Fall Time:**

|  |  |  |
| --- | --- | --- |
| **Drive Strength** | **Min. (nS)** | **Max. (nS)** |
| BUFX2 | 0.204083 | 3.555283 |
| BUFX4 | 0.195164 | 4.338193 |
| BUFX8 | 0.184735 | 4.346652 |

**Output Rise Time:**

|  |  |  |
| --- | --- | --- |
| **Drive Strength** | **Min. (nS)** | **Max. (nS)** |
| BUFX2 | 0.200962 | 3.287624 |
| BUFX4 | 0.24433 | 3.139659 |
| BUFX8 | 0.185384 | 3.129319 |

**Logic Symbol:**

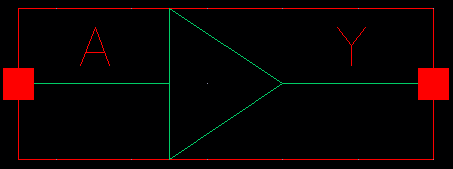
****

Figure 1: Symbol View for the buffer cell.

**CMOS Schematic:**The following figures display the CMOS schematics for the BUF cells.

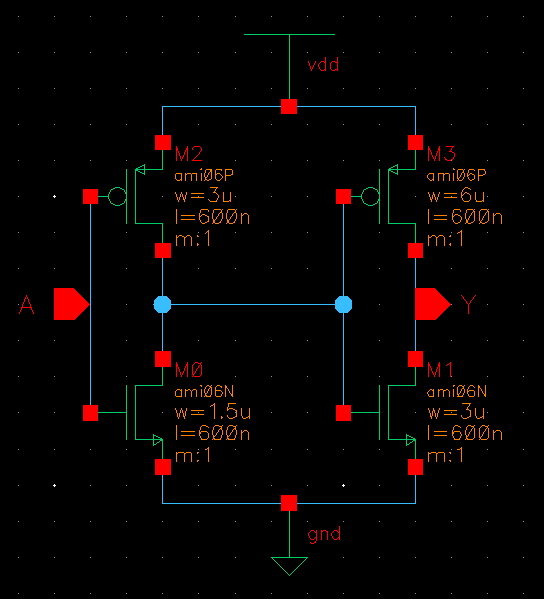
****

Figure 2: CMOS Schematic for the BUFX2 cell.

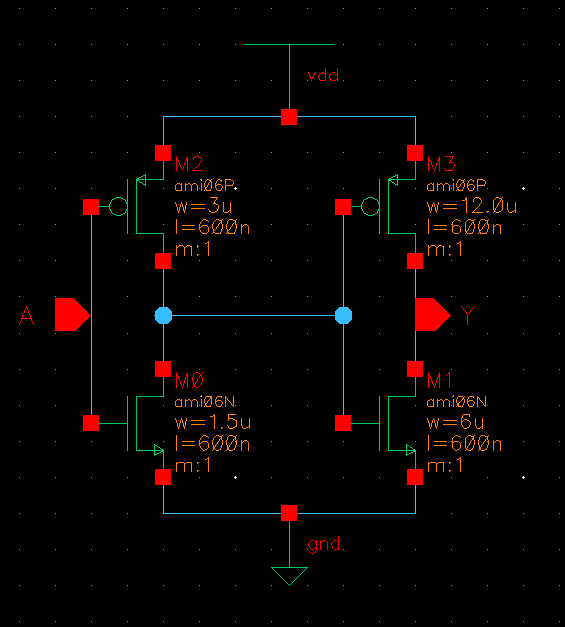


Figure 3: CMOS Schematic for the BUFX2 cell.

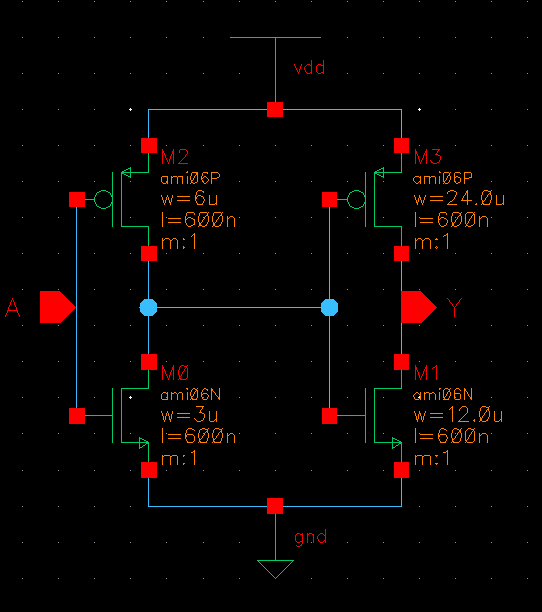


Figure 4: CMOS Schematic for the BUFX8 cell.

**CMOS Layout:**

The following figures display the CMOS layouts for the BUF cells.

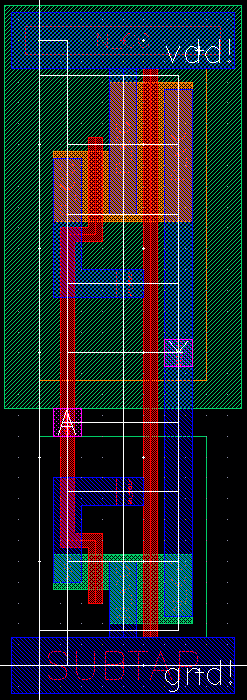
****

Figure 5: CMOS layout for the BUFX2 cell.

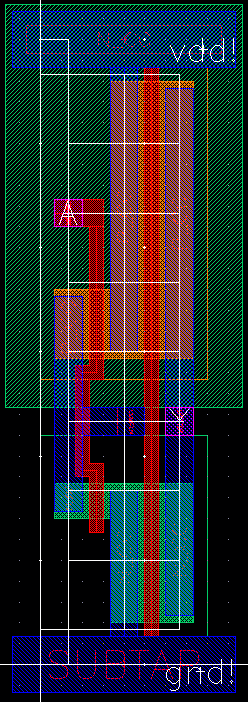
****

Figure 6: CMOS layout for the BUFX4 cell.

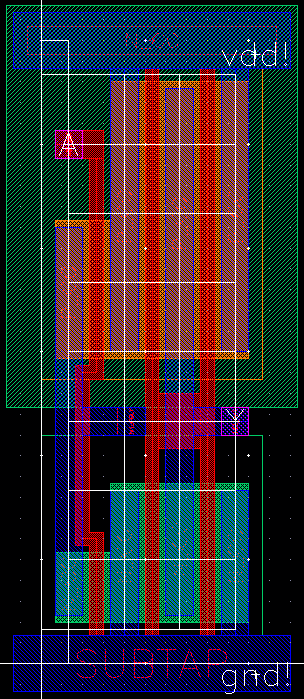
****

Figure 7: CMOS layout for the BUFX8 cell.

# DFF

**Cell Description:**This is a standard single-bit, positive-edge triggered flip-flop with an asynchronous, active low clear signal. The input signal to this cell is sampled on the rising edge of the clock signal, and both the sampled signal and its compliment are provided at the output of the cell.

**Truth Table:**

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| **CLK** | **D** | **CLRBAR** | **Q** |  |
| 0 | 0 | 0 | 0 |  |
| 0 | 0 | 1 | Q |  |
| 0 | 1 | 0 | 0 |  |
| 0 | 1 | 1 | Q |  |
| 1 | 0 | 0 | 0 | 1 |
| 1 | 0 | 1 | 0 | 1 |
| 1 | 1 | 0 | 0 | 1 |
| 1 | 1 | 1 | 1 | 0 |

**Behavioral Verilog:**

//Verilog HDL for "Lib6710\_06", "DFF" "behavioral"

module DFF ( Q, QB, CLRB, CLK, D );

input CLRB;

input CLK;

input D;

output reg Q;

output QB;

assign QB = ~Q;

always@(posedge CLK or negedge CLRB)

begin

if(~CLRB)

Q <= 1'b0;

else

Q <= D;

end

specify

(D => Q) = (1.0, 1.0);

(D => QB) = (1.0, 1.0);

(CLK => Q) = (1.0, 1.0);

(CLK => QB) = (1.0, 1.0);

(CLRB => Q) = (1.0, 1.0);

(CLRB => QB) = (1.0, 1.0);

endspecify

endmodule

**Cell Size:**

|  |  |  |
| --- | --- | --- |
| **Drive Strength** | **Height (μM)** | **Width (μM)** |
| DFFX1 | 27.0 | 48 |

**Performance:**

**Propagation Delay (Rising Outputs):**

|  |  |  |
| --- | --- | --- |
| **Drive Strength** | **Min.** | **Max.** |
| DFFX1 |  |  |

**Propagation Delay (Falling Outputs):**

|  |  |  |
| --- | --- | --- |
| **Drive Strength** | **Min.** | **Max.** |
| DFFX1 |  |  |

**Output Fall Time:**

|  |  |  |
| --- | --- | --- |
| **Drive Strength** | **Min.** | **Max.** |
| DFFX1 |  |  |

**Output Rise Time:**

|  |  |  |
| --- | --- | --- |
| **Drive Strength** | **Min.** | **Max.** |
| DFFX1 |  |  |

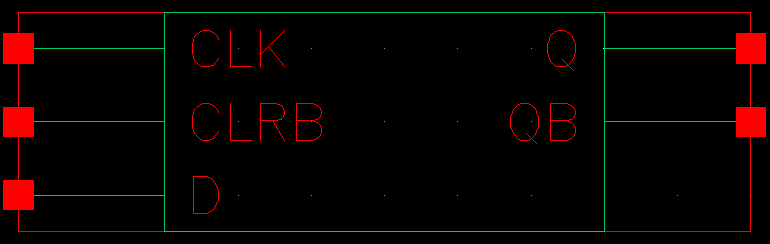
**Logic Symbol:  
**

Figure 1: Symbol View for the DFF cell.

**CMOS Schematic:**

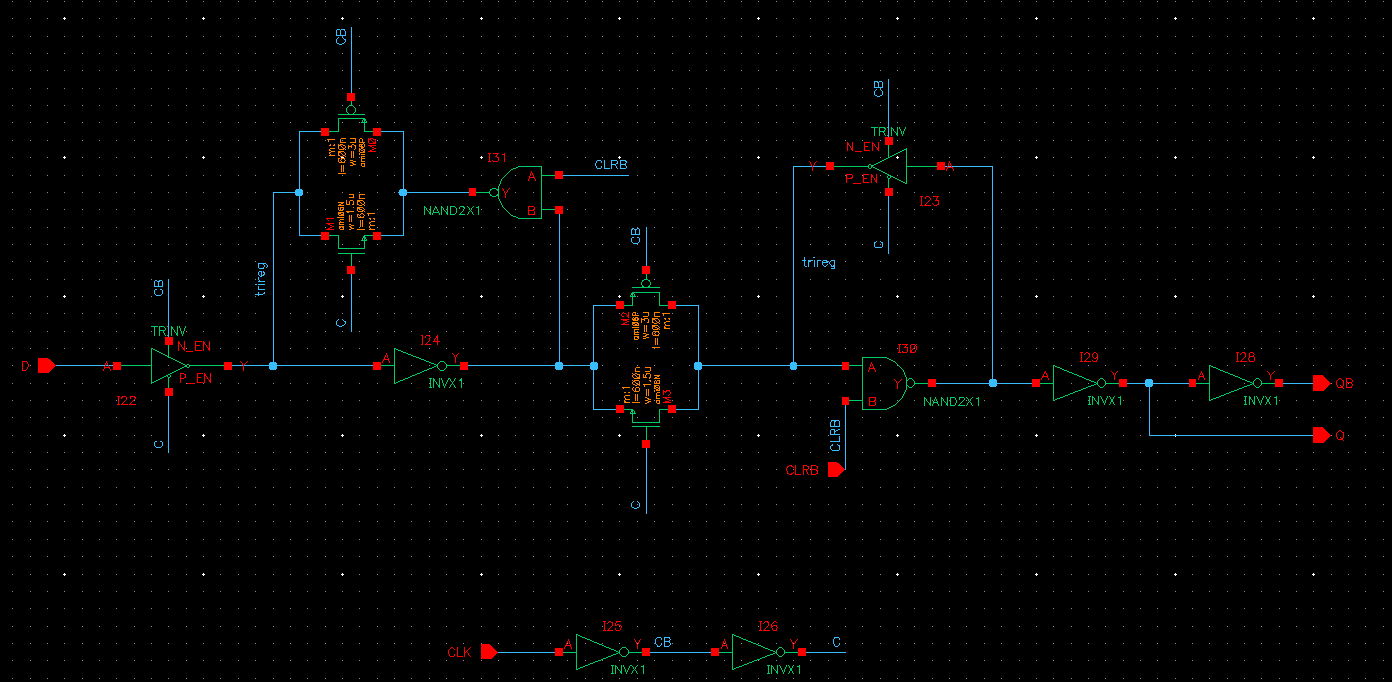
****

Figure 2: CMOS schematic for the DFFX1 Cell

**CMOS Layout:**

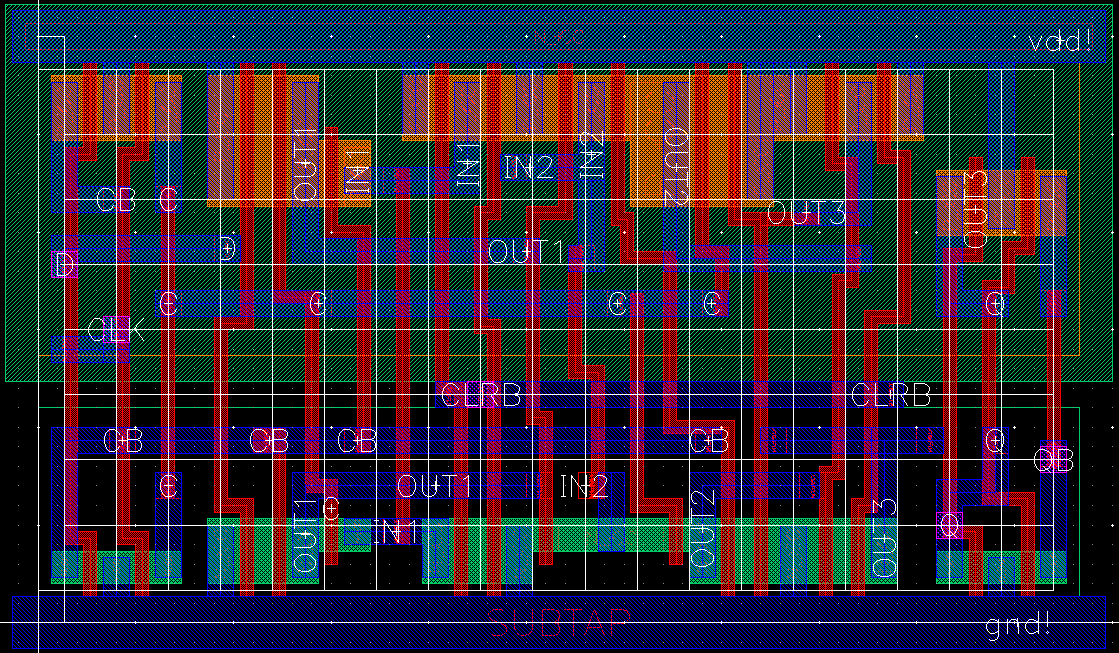
****

Figure 3: CMOS layout for the DFFX1 cell.

# DFFNEGCLK

**Cell Description:**This is a standard single-bit, negative-edge triggered flip-flop with an asynchronous, active low clear signal. The input signal to this cell is sampled on the falling edge of the clock signal, and both the sampled signal and its compliment are provided at the output of the cell.

**Truth Table:**

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| **CLK** | **D** | **CLRBAR** | **Q** |  |
| 0 | 0 | 0 | 0 |  |
| 0 | 0 | 1 | 0 |  |
| 0 | 1 | 0 | 1 |  |
| 0 | 1 | 1 | Q |  |
| 1 | 0 | 0 | 0 | 1 |
| 1 | 0 | 1 | Q |  |
| 1 | 1 | 0 | 0 | 1 |
| 1 | 1 | 1 | Q |  |

**Behavioral Verilog:**

//Verilog HDL for "Lib6710\_06", "DFFNEGCLK" "behavioral"

module DFFNEGCLK( Q, QB, CLRB, CLK, D );

input CLRB;

input CLK;

input D;

output reg Q;

output QB;

assign QB = ~Q;

always@(negedge CLK or negedge CLRB)

begin

if(~CLRB)

Q <= 1'b0;

else

Q <= D;

end

specify

(D => Q) = (1.0, 1.0);

(D => QB) = (1.0, 1.0);

(CLK => Q) = (1.0, 1.0);

(CLK => QB) = (1.0, 1.0);

(CLRB => Q) = (1.0, 1.0);

(CLRB => QB) = (1.0, 1.0);

endspecify

endmodule

**Cell Size:**

|  |  |  |
| --- | --- | --- |
| **Drive Strength** | **Height (μM)** | **Width (μM)** |
| DFFNEGCLKX1 | 27.0 | 48 |

**Performance:**

**Propagation Delay (Rising Outputs):**

|  |  |  |
| --- | --- | --- |
| **Drive Strength** | **Min.** | **Max.** |
| DFFNEGCLKX1 |  |  |

**Propagation Delay (Falling Outputs):**

|  |  |  |
| --- | --- | --- |
| **Drive Strength** | **Min.** | **Max.** |
| DFFNEGCLKX1 |  |  |

**Output Fall Time:**

|  |  |  |
| --- | --- | --- |
| **Drive Strength** | **Min.** | **Max.** |
| DFFNEGCLKX1 |  |  |

**Output Rise Time:**

|  |  |  |
| --- | --- | --- |
| **Drive Strength** | **Min.** | **Max.** |
| DFFNEGCLKX1 |  |  |

**Logic Symbol:**

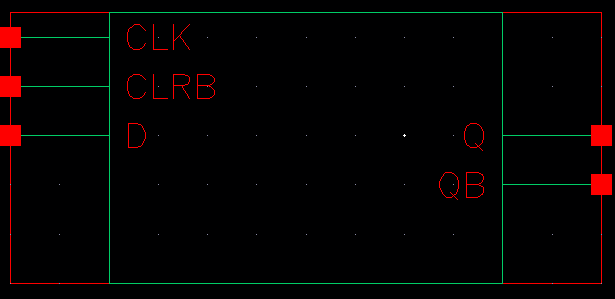
****

Figure 1: Symbol View for the DFFNEGCLK cell.

**CMOS Schematic:**

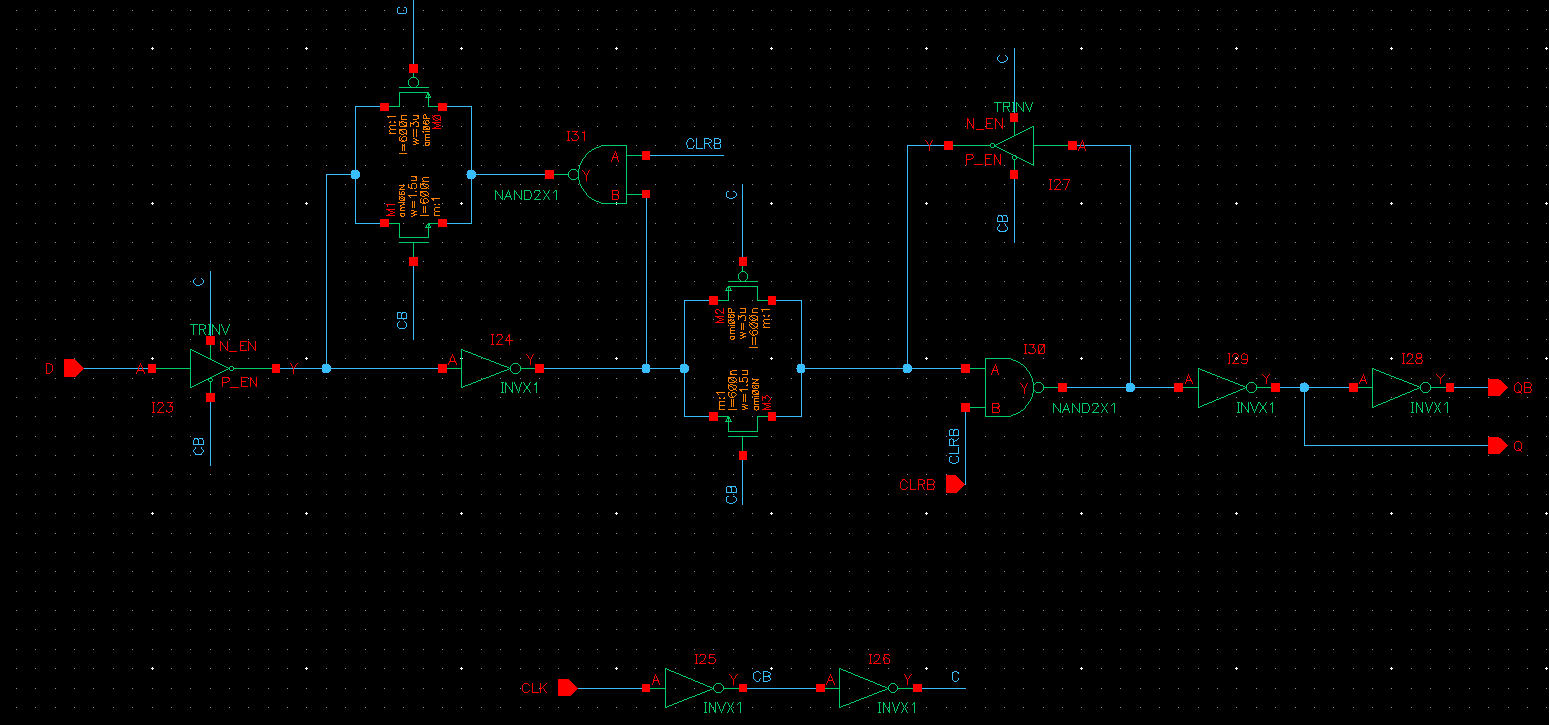
****

Figure 2: CMOS schematic for the DFFNEGCLKX1 Cell

**CMOS Layout:**

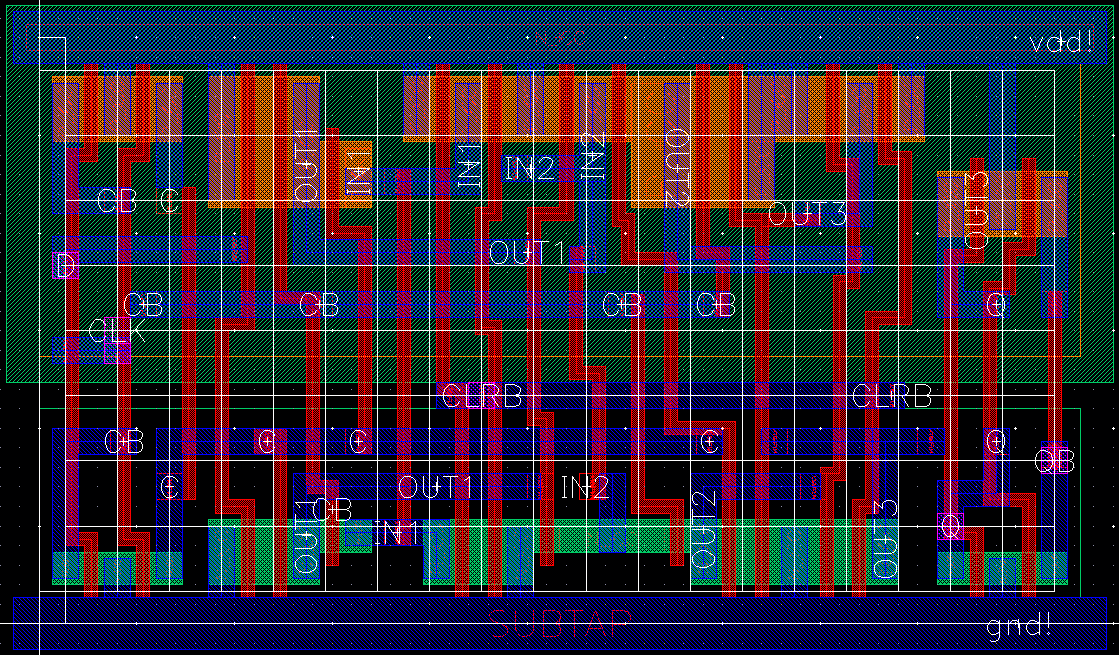
****

Figure 3: CMOS layout for the DFFNEGCLKX1 cell.

# DFFQ

**Cell Description:**This is a standard single-bit, positive-edge triggered flip-flop with an asynchronous, active low clear signal. The input signal to this cell is sampled on the rising edge of the clock signal, only the sampled signal is available at the output of the cell.

**Truth Table:**

|  |  |  |  |
| --- | --- | --- | --- |
| **CLK** | **D** | **CLRBAR** | **Q** |
| 0 | 0 | 0 | 0 |
| 0 | 0 | 1 | Q |
| 0 | 1 | 0 | 0 |
| 0 | 1 | 1 | Q |
| 1 | 0 | 0 | 0 |
| 1 | 0 | 1 | 0 |
| 1 | 1 | 0 | 0 |
| 1 | 1 | 1 | 1 |

**Behavioral Verilog:**

//Verilog HDL for "Lib6710\_06", "DFF" "behavioral"

module DFFQ( Q, CLRB, CLK, D );

input CLRB;

input CLK;

input D;

output reg Q;

always@(posedge CLK or negedge CLRB)

begin

if(~CLRB)

Q <= 1'b0;

else

Q <= D;

end

specify

(D => Q) = (1.0, 1.0);

(CLK => Q) = (1.0, 1.0);

(CLRB => Q) = (1.0, 1.0);

endspecify

endmodule

**Cell Size:**

|  |  |  |
| --- | --- | --- |
| **Drive Strength** | **Height (μM)** | **Width (μM)** |
| DFFQX1 | 27.0 | 45.6 |

**Performance:**

**Propagation Delay (Rising Outputs):**

|  |  |  |
| --- | --- | --- |
| **Drive Strength** | **Min.** | **Max.** |
| DFFQX1 |  |  |

**Propagation Delay (Falling Outputs):**

|  |  |  |
| --- | --- | --- |
| **Drive Strength** | **Min.** | **Max.** |
| DFFQX1 |  |  |

**Output Fall Time:**

|  |  |  |
| --- | --- | --- |
| **Drive Strength** | **Min.** | **Max.** |
| DFFQX1 |  |  |

**Output Rise Time:**

|  |  |  |
| --- | --- | --- |
| **Drive Strength** | **Min.** | **Max.** |
| DFFQX1 |  |  |

**Logic Symbol:**

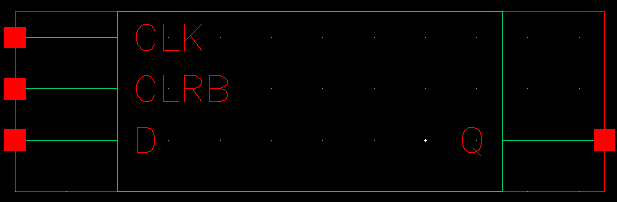
****

Figure 1: Symbol View for the DFFQ cell.

**CMOS Schematic:**

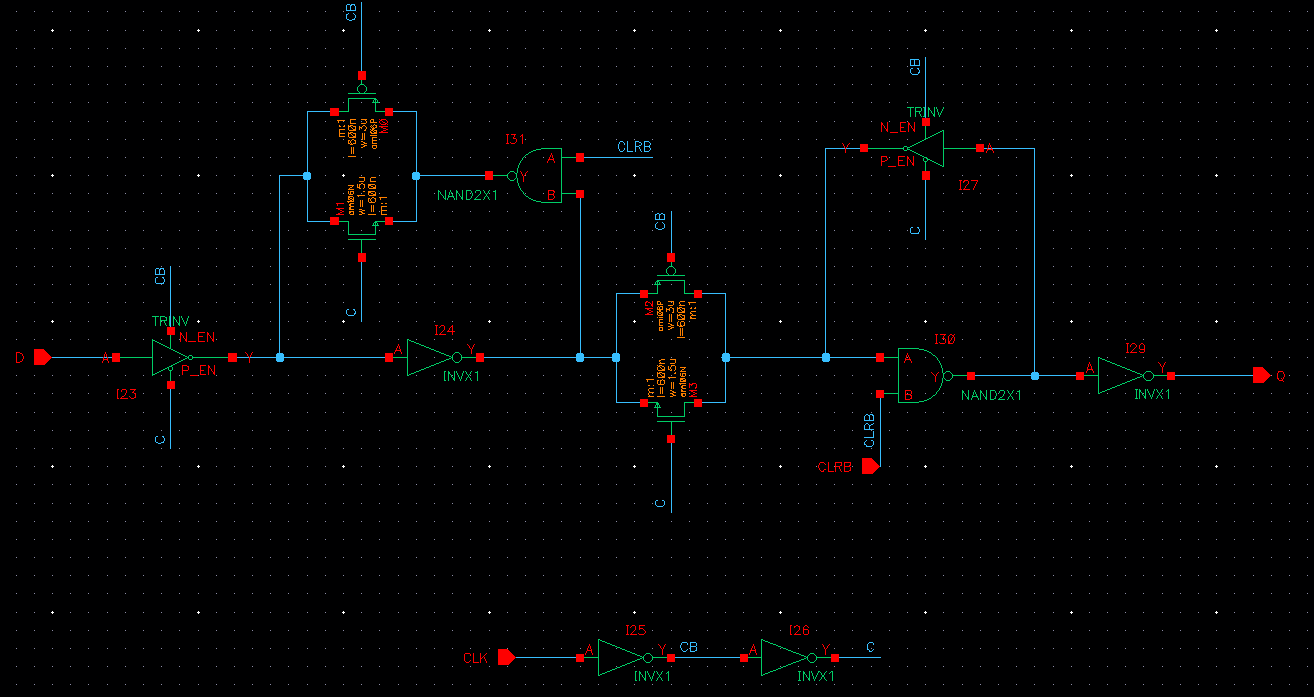
****

Figure 2: CMOS schematic for the DFFQX1 Cell

**CMOS Layout:**

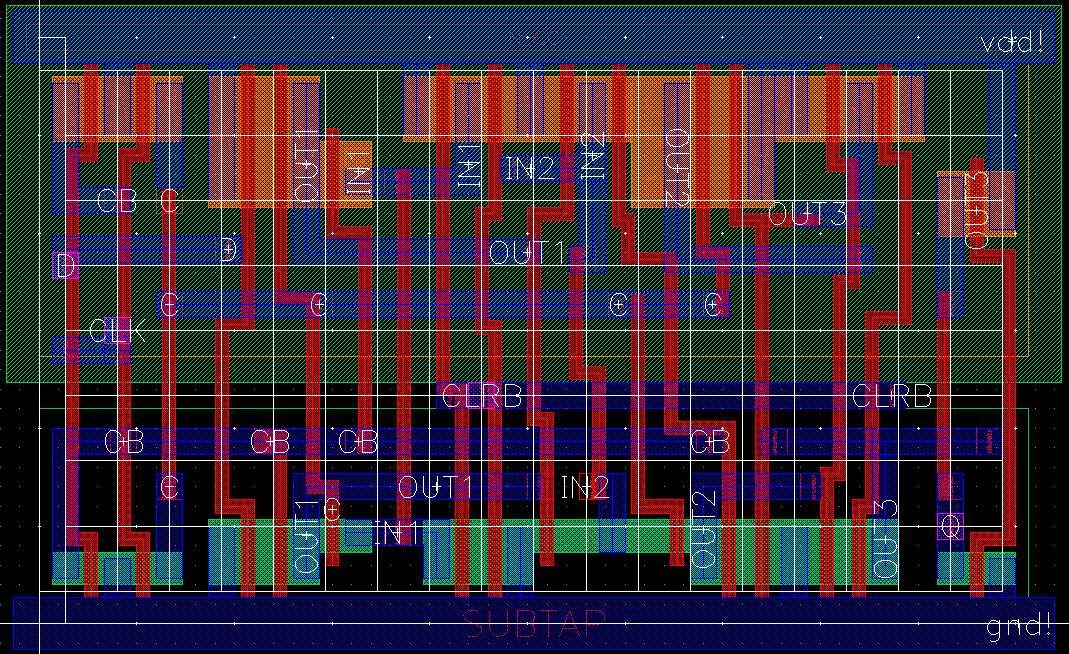
****

Figure 3: CMOS layout for the DFFQX1 cell.

# DFFQB

**Cell Description:**This is a standard single-bit, positive-edge triggered flip-flop with an asynchronous, active low clear signal. The input signal to this cell is sampled on the rising edge of the clock signal, only the compliment of the sampled signal is available at the output of the cell.

**Truth Table:**

|  |  |  |  |
| --- | --- | --- | --- |
| **CLK** | **D** | **CLRBAR** |  |
| 0 | 0 | 0 | 0 |
| 0 | 0 | 1 |  |
| 0 | 1 | 0 | 0 |
| 0 | 1 | 1 |  |
| 1 | 0 | 0 | 0 |
| 1 | 0 | 1 | 1 |
| 1 | 1 | 0 | 0 |
| 1 | 1 | 1 | 0 |

**Behavioral Verilog:**

//Verilog HDL for "Lib6710\_06", "DFF" "behavioral"

module DFFQB( QB, CLRB, CLK, D );

input CLRB;

input CLK;

input D;

output reg QB;

always@(posedge CLK or negedge CLRB)

begin

if(~CLRB) //Active low clear

QB <= 1'b1;

else

QB <= ~D;

end

specify

(D => QB) = (1.0, 1.0);

(CLK => QB) = (1.0, 1.0);

(CLRB => QB) = (1.0, 1.0);

endspecify

endmodule

**Cell Size:**

|  |  |  |
| --- | --- | --- |
| **Drive Strength** | **Height (μM)** | **Width (μM)** |
| DFFQBX1 | 27.0 | 48 |

**Performance:**

**Propagation Delay (Rising Outputs):**

|  |  |  |
| --- | --- | --- |
| **Drive Strength** | **Min.** | **Max.** |
| DFFQBX1 |  |  |

**Propagation Delay (Falling Outputs):**

|  |  |  |
| --- | --- | --- |
| **Drive Strength** | **Min.** | **Max.** |
| DFFQBX1 |  |  |

**Output Fall Time:**

|  |  |  |
| --- | --- | --- |
| **Drive Strength** | **Min.** | **Max.** |
| DFFQBX1 |  |  |

**Output Rise Time:**

|  |  |  |
| --- | --- | --- |
| **Drive Strength** | **Min.** | **Max.** |
| DFFQBX1 |  |  |

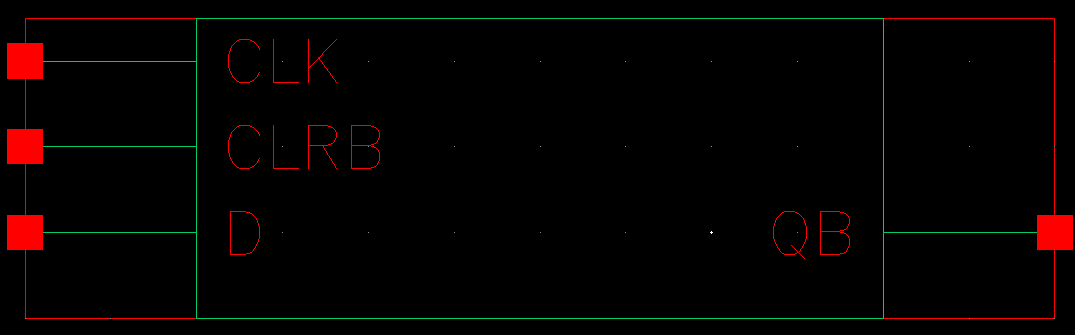
**Logic Symbol:  
**

Figure 1: Symbol View for the DFFQB cell.

**CMOS Schematic:**

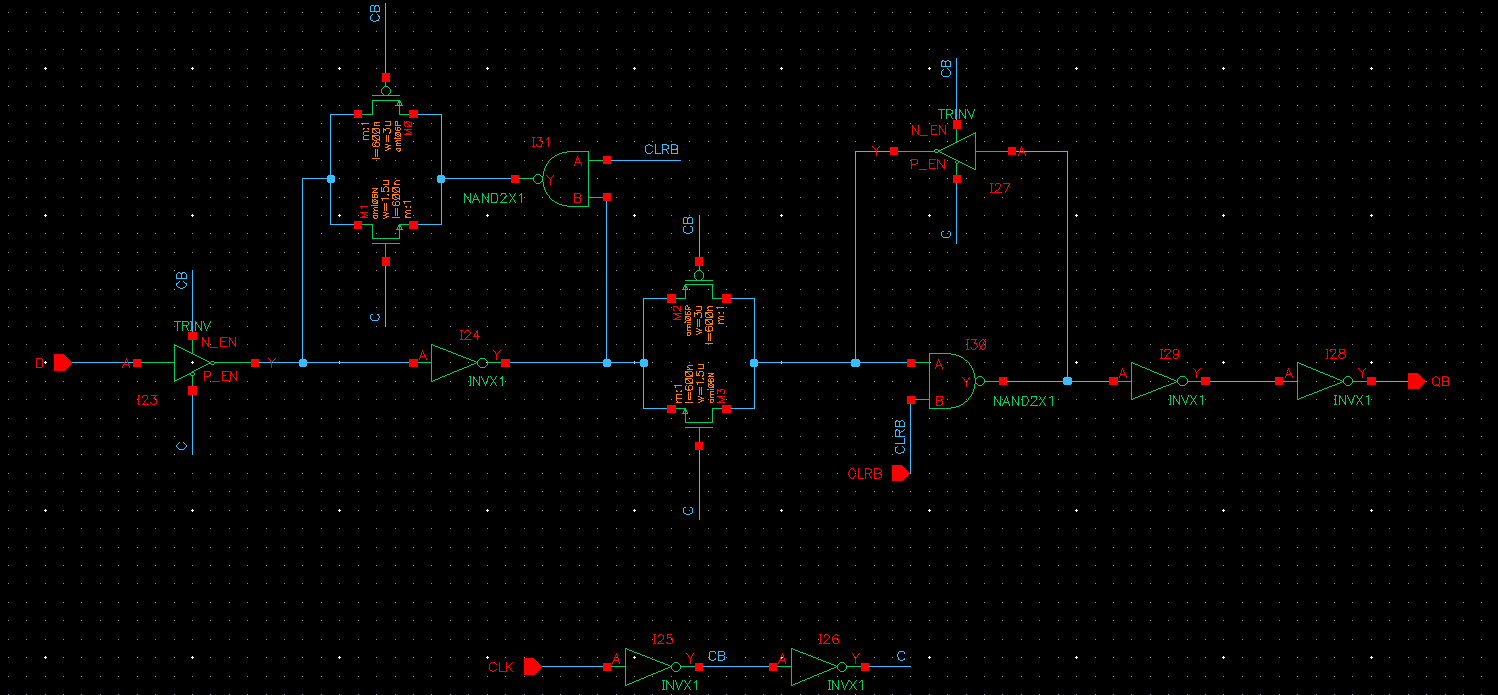
****

Figure 2: CMOS schematic for the DFFQBX1 Cell

**CMOS Layout:**

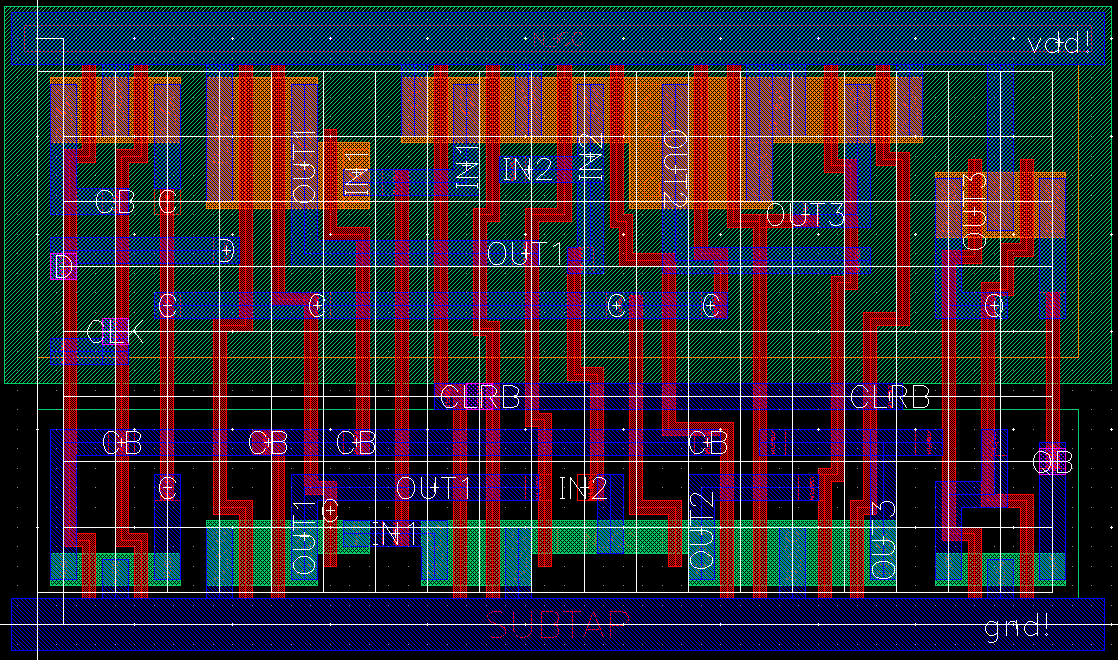
****

Figure 3: CMOS layout for the DFFQBX1 cell.

# INV

**Cell Description:**

This is a standard inverter cell with the following Boolean equation.

**Truth Table:**

|  |  |
| --- | --- |
| A | Y |
| 0 | 1 |
| 1 | 0 |

**Behavioral Verilog:**

The behavioral Verilog for the inverter is independent of its drive strength. Replace the N in the module name with the respective drive strength (i.e. 1, 2, 4, and 8).

//Verilog HDL for "Lib6710\_06", "INVXN" "behavioral"

module INVXN ( Y, A );

output Y;

input A;

not \_i0(Y, A);

specify

(A => Y) = (1.0, 1.0);

endspecify

endmodule

**Cell Size:**

|  |  |  |
| --- | --- | --- |
| **Drive Strength** | **Height (μM)** | **Width (μM)** |
| INVX1 | 27.0 | 4.8 |
| INVX2 | 27.0 | 4.8 |
| INVX4 | 27.0 | 4.8 |
| INVX8 | 27.0 | 7.2 |

**Performance:**

**Propagation Delay (Rising Outputs):**

|  |  |  |
| --- | --- | --- |
| **Drive Strength** | **Min. (nS)** | **Max. (nS)** |
| INVX1 | 0.261011 | 4.441372 |
| INVX2 | 0.225636 | 4.087162 |
| INVX4 | 0.20974 | 3.927988 |
| INVX8 | 0.19849 | 3.197132 |

**Propagation Delay (Falling Outputs):**

|  |  |  |
| --- | --- | --- |
| **Drive Strength** | **Min. (nS)** | **Max. (nS)** |
| INVX1 | 0.353699 | 5.887184 |
| INVX2 | 0.257917 | 4.566927 |
| INVX4 | 0.233438 | 4.095382 |
| INVX8 | 0.210379 | 4.073315 |

**Output Fall Time:**

|  |  |  |
| --- | --- | --- |
| **Drive Strength** | **Min. (nS)** | **Max. (nS)** |
| INVX1 | 0.267747 | 4.725145 |
| INVX2 | 0.185996 | 3.561277 |
| INVX4 | 0.156828 | 3.151193 |
| INVX8 | 0.145615 | 3.129725 |

**Output Rise Time:**

|  |  |  |
| --- | --- | --- |
| **Drive Strength** | **Min. (nS)** | **Max. (nS)** |
| INVX1 | 0.208141 | 3.634253 |
| INVX2 | 0.173378 | 3.283945 |
| INVX4 | 0.157781 | 3.127143 |
| INVX8 | 0.14623 | 3.115807 |

**Logic Symbol**

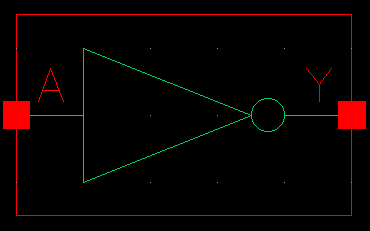
****

Figure 1: Symbol View for the inverter cell.

**CMOS Schematic**The following figure displays the CMOS schematic for the invert cell with a 1 times drive strength (INVX1), all drive strengths have the same schematic with transistor widths that scale by the drive strength factor (i.e. the width of the PMOS in the INVX2 is 6.0μM and the NMOS width is 3.0μM) .

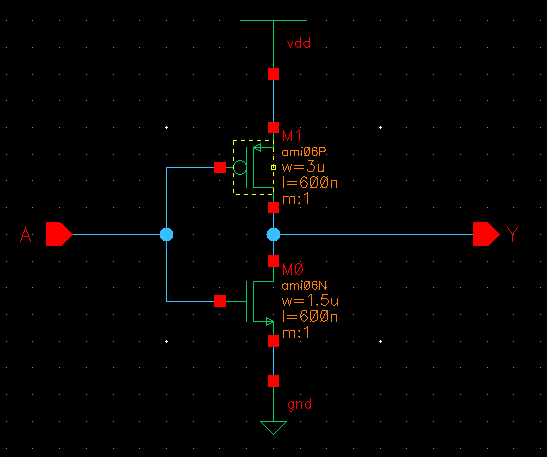
****

Figure 2: CMOS Schematic for the INVX1 cell.

**CMOS Layout:**The following figures display the CMOS layouts for the INV cells.

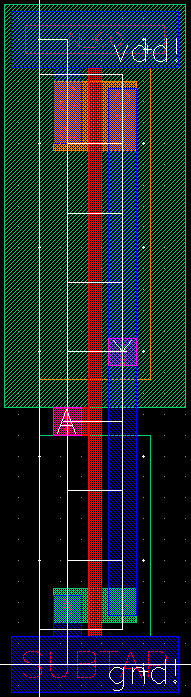
****

Figure 3: CMOS layout for the INVX1 cell.

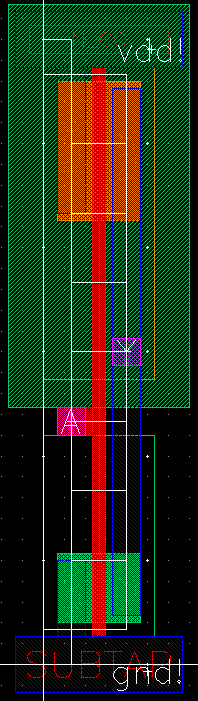
****

Figure 4: CMOS layout for the INVX2 cell.

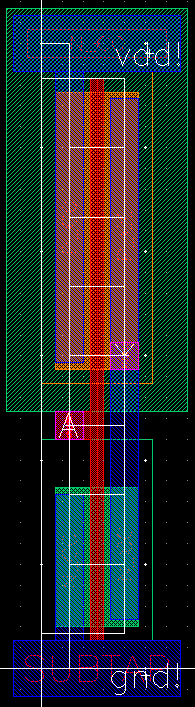
****

Figure 5: CMOS layout for the INVX4 cell.

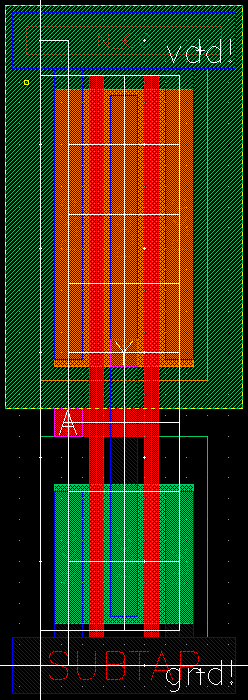
****

Figure 6:CMOS layout for the INVX8 cell.

# MUXINV

**Cell Description:**This is a standard 2 input multiplexor with an inverted output cell described by the following Boolean equation.

**Truth Table:**

|  |  |  |  |
| --- | --- | --- | --- |
| **S** | **A** | **B** | **Y** |
| 0 | 0 | 0 | 1 |
| 0 | 0 | 1 | 1 |
| 0 | 1 | 0 | 0 |
| 0 | 1 | 1 | 0 |
| 1 | 0 | 0 | 1 |
| 1 | 0 | 1 | 0 |
| 1 | 1 | 0 | 1 |
| 1 | 1 | 1 | 0 |

**Behavioral Verilog:**

//Verilog HDL for "Lib6710\_06", "MUXINV2x1" "behavioral"

module MUXINV2X1( Y, A, B, S );

input A;

input S;

output Y;

input B;

assign Y = ~((~S&A) | (S&B));

specify

(A => Y) = (1.0, 1.0);

(B => Y) = (1.0, 1.0);

(S => Y) = (1.0, 1.0);

endspecify

endmodule

**Cell Size:**

|  |  |  |
| --- | --- | --- |
| **Drive Strength** | **Height (μM)** | **Width (μM)** |
| MUXINV2X1 | 27.0 | 14.4 |

**Performance:**

**Propagation Delay (Rising Outputs):**

|  |  |  |
| --- | --- | --- |
| **Drive Strength** | **Min. (nS)** | **Max. (nS)** |
| MUXINV2X1 | 0.331604 | 4.139029 |

**Propagation Delay (Falling Outputs):**

|  |  |  |
| --- | --- | --- |
| **Drive Strength** | **Min. (nS)** | **Max. (nS)** |
| MUXINV2X1 | 0.33067 | 3.905376 |

**Output Fall Time:**

|  |  |  |
| --- | --- | --- |
| **Drive Strength** | **Min. (nS)** | **Max. (nS)** |
| MUXINV2X1 | 0.248249 | 3.015543 |

**Output Rise Time:**

|  |  |  |
| --- | --- | --- |
| **Drive Strength** | **Min. (nS)** | **Max. (nS)** |
| MUXINV2X1 | 0.275295 | 3.230027 |

**Logic Symbol:**

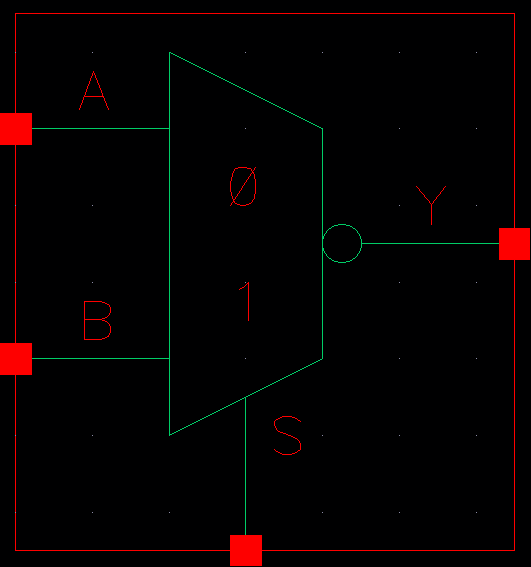
****

Figure 1: Symbol View for the MUXINV cell.

**CMOS Schematic:**

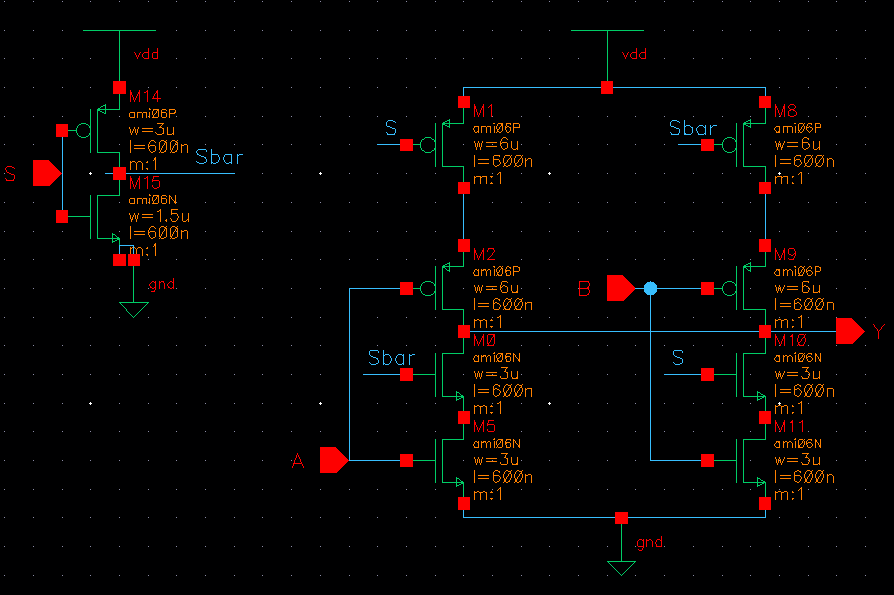
****

Figure 2: CMOS Schematic for the MUXINV2X1 cell.

**CMOS Layout:**

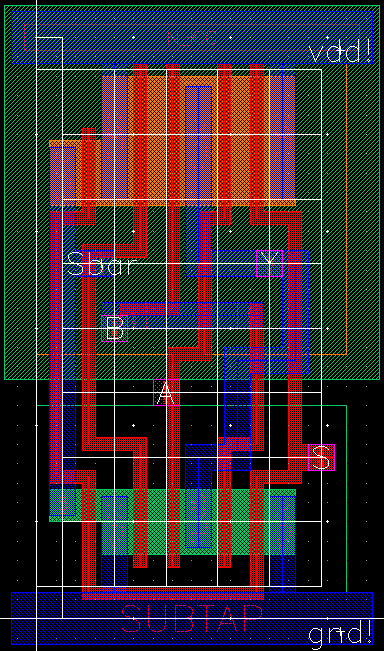
****

Figure 3: CMOS layout for the MUXINV2X1 cell.

# NAND

**Cell Description:**This is a standard NAND cell with the following Boolean equation.

**Truth Table:**

|  |  |  |
| --- | --- | --- |
| **A** | **B** | **Y** |
| 0 | 0 | 1 |
| 0 | 1 | 1 |
| 1 | 0 | 1 |
| 1 | 1 | 0 |

**Behavioral Verilog:**The behavioral Verilog for the NAND is independent of its drive strength. Replace the N in the module name with the respective drive strength (i.e. 1, 2).

//Verilog HDL for "Lib6710\_06", "NAND2X1" "behavioral"

module NAND2X1 ( Y, A, B );

output Y;

input A;

input B;

nand \_i0(Y, A, B);

specify

(A => Y) = (1.0, 1.0);

(B => Y) = (1.0, 1.0);

endspecify

endmodule

**Cell Size:**

|  |  |  |
| --- | --- | --- |
| **Drive Strength** | **Height (μM)** | **Width (μM)** |
| NAND2X1 | 27.0 | 7.2 |
| NAND2X2 | 27.0 | 7.2 |

**Performance:**

**Propagation Delay (Rising Outputs):**

|  |  |  |
| --- | --- | --- |
| **Drive Strength** | **Min. (nS)** | **Max. (nS)** |
| NAND2X1 | 0.287135 | 4.512479 |
| NAND2X2 | 0.24711 | 4.144368 |

**Propagation Delay (Falling Outputs):**

|  |  |  |
| --- | --- | --- |
| **Drive Strength** | **Min. (nS)** | **Max. (nS)** |
| NAND2X1 | 0.239633 | 3.695076 |
| NAND2X2 | 0.200718 | 3.297926 |

**Output Fall Time:**

|  |  |  |
| --- | --- | --- |
| **Drive Strength** | **Min. (nS)** | **Max. (nS)** |
| NAND2X1 | 0.182966 | 2.933345 |
| NAND2X2 | 0.148407 | 2.57788 |

**Output Rise Time:**

|  |  |  |
| --- | --- | --- |
| **Drive Strength** | **Min. (nS)** | **Max. (nS)** |
| NAND2X1 | 0.221013 | 3.676704 |
| NAND2X2 | 0.183531 | 3.321374 |

**Logic Symbol:**

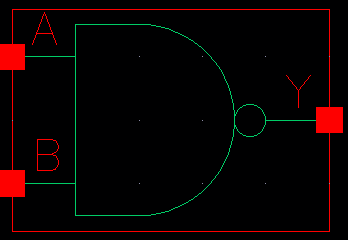
****

Figure 1: Symbol View for the NAND cell.

**CMOS Schematic:**The following figure displays the CMOS schematic for the NAND cell with a 1 times drive strength (NAND2X1), all drive strengths have the same schematic with transistor widths that scale by the drive  
 strength factor (i.e. the width of the PMOS in the NAND2X2 is 6.0μM and the NMOS width is 6.0μM) .

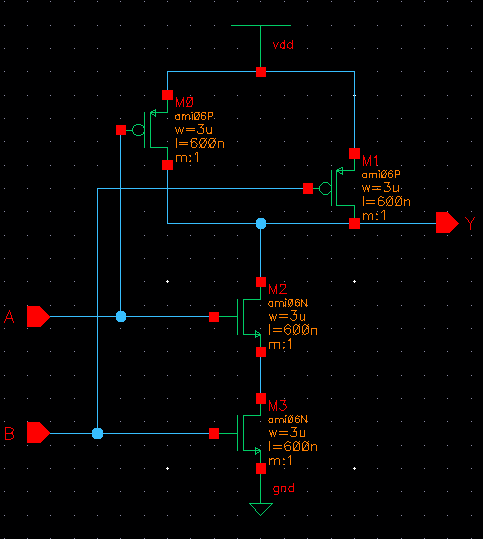


Figure 2: CMOS Schematic for the NAND2X1 cell.

**CMOS Layout:**

The following figures display the CMOS layouts for the NAND cells.



Figure 3: CMOS layout for the NAND2X1 cell.



Figure 4: CMOS layout for the NAND2X2 cell.

# NOR

**Cell Description:**

This is a standard NOR cell with the following Boolean equation.

**Truth Table:**

|  |  |  |
| --- | --- | --- |
| **A** | **B** | **Y** |
| 0 | 0 | 1 |
| 0 | 1 | 0 |
| 1 | 0 | 0 |
| 1 | 1 | 0 |

**Behavioral Verilog:**

The behavioral Verilog for the NOR is independent of its drive strength. Replace the N in the module name with the respective drive strength (i.e. 1, 2).

//Verilog HDL for "Lib6710\_06", "NOR2X2" "behavioral"

module NOR2X2 ( Y, A, B );

input A;

output Y;

input B;

nor \_i0(Y, A, B);

specify

(A => Y) = (1.0, 1.0);

(B => Y) = (1.0, 1.0);

endspecify

endmodule

**Cell Size:**

|  |  |  |
| --- | --- | --- |
| **Drive Strength** | **Height (μM)** | **Width (μM)** |
| NOR2X1 | 27.0 | 7.2 |
| NOR2X1 | 27.0 | 7.2 |

**Performance:**

**Propagation Delay (Rising Outputs):**

|  |  |  |
| --- | --- | --- |
| **Drive Strength** | **Min.** | **Max.** |
| NOR2X1 | **0.264909** | **3.863364** |
| NOR2X1 | **0.233628** | **3.703823** |

**Propagation Delay (Falling Outputs):**

|  |  |  |
| --- | --- | --- |
| **Drive Strength** | **Min.** | **Max.** |
| NOR2X1 | **0.428223** | **6.032361** |
| NOR2X1 | **0.304294** | **4.673979** |

**Output Fall Time:**

|  |  |  |
| --- | --- | --- |
| **Drive Strength** | **Min.** | **Max.** |
| NOR2X1 | **0.294217** | **4.824453** |
| NOR2X1 | **0.202087** | **3.63339** |

**Output Rise Time:**

|  |  |  |
| --- | --- | --- |
| **Drive Strength** | **Min.** | **Max.** |
| NOR2X1 | **0.214311** | **3.165392** |
| NOR2X1 | **0.187695** | **3.003025** |

**Logic Symbol:**

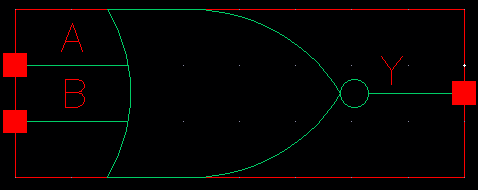
****

Figure 1: Symbol View for the NOR cell.

**CMOS Schematic:**

The following figures display the CMOS schematics for the NOR cells.

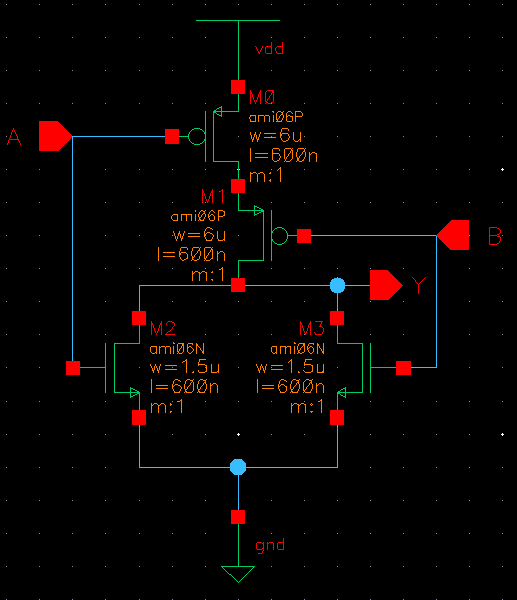


Figure 2: CMOS Schematic for the NOR2X1 cell.

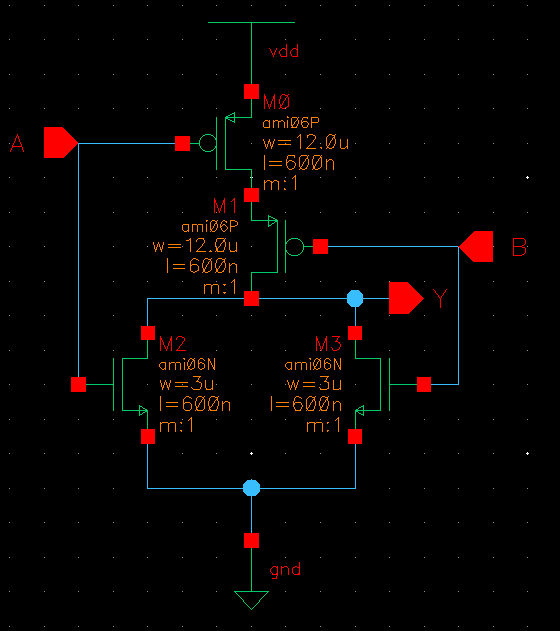


Figure 3: CMOS Schematic for the NOR2X2 cell.

**CMOS Layout:**

The following figures display the CMOS layouts for the NOR cells.

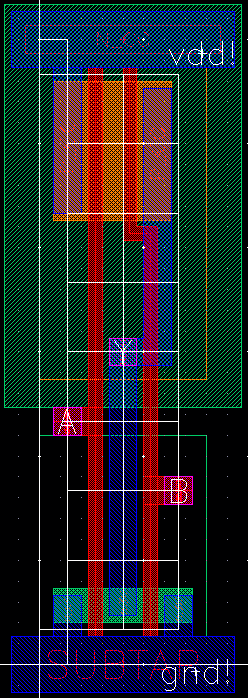
****

Figure 4: CMOS layout for the NOR2X1 cell.

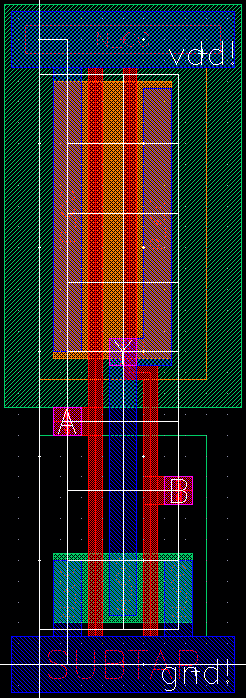
****

Figure 5: CMOS layout for the NOR2X2 cell.

# OAI21

**Cell Description:**This is a standard 3 input OR AND INVERT (OAI) cell. This cells functionality is described by the following Boolean equation:

**Truth Table:**

|  |  |  |  |
| --- | --- | --- | --- |
| **A** | **B** | **C** | **Y** |
| 0 | 0 | 0 | 1 |
| 0 | 0 | 1 | 1 |
| 0 | 1 | 0 | 1 |
| 0 | 1 | 1 | 1 |
| 1 | 0 | 0 | 1 |
| 1 | 0 | 1 | 1 |
| 1 | 1 | 0 | 1 |
| 1 | 1 | 1 | 0 |

**Behavioral Verilog:**

//Verilog HDL for "Lib6710\_06", "OAI21X1" "behavioral"

module OAI21X1 ( Y, A, B, C );

input A;

input C;

output Y;

input B;

assign Y = ~((A | B) & C);

specify

(A => Y) = (1.0, 1.0);

(B => Y) = (1.0, 1.0);

(C => Y) = (1.0, 1.0);

endspecify

endmodule

**Cell Size:**

|  |  |  |
| --- | --- | --- |
| **Drive Strength** | **Height (μM)** | **Width (μM)** |
| OAI21X1 | 27.0 | 9.6 |

**Performance:**

**Propagation Delay (Rising Outputs):**

|  |  |  |
| --- | --- | --- |
| **Drive Strength** | **Min.** | **Max.** |
| OAI21X1 |  |  |

**Propagation Delay (Falling Outputs):**

|  |  |  |
| --- | --- | --- |
| **Drive Strength** | **Min.** | **Max.** |
| OAI21X1 |  |  |

**Output Fall Time:**

|  |  |  |
| --- | --- | --- |
| **Drive Strength** | **Min.** | **Max.** |
| OAI21X1 |  |  |

**Output Rise Time:**

|  |  |  |
| --- | --- | --- |
| **Drive Strength** | **Min.** | **Max.** |
| OAI21X1 |  |  |

**Logic Symbol:**

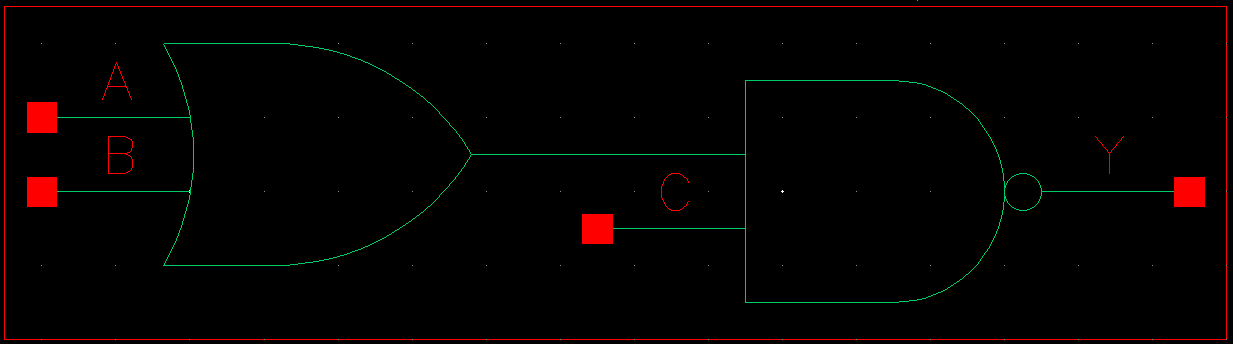
****

Figure 1: Symbol View for the OAI21 cell

**CMOS Schematic:**

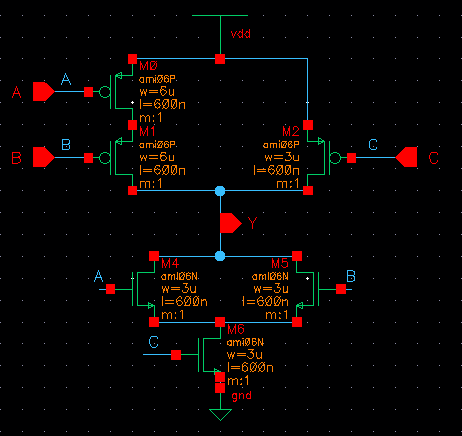
****

Figure 2: CMOS schematic view for the AOI21X1 cell.

**CMOS Layout:**

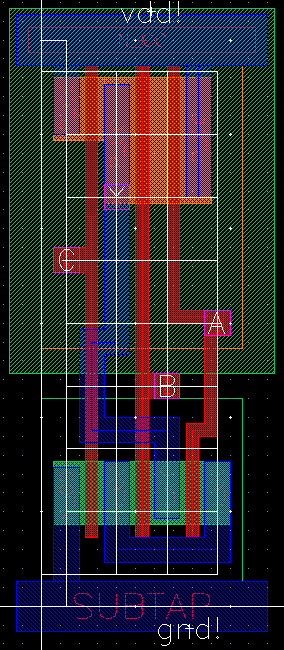
****

Figure 3: CMOS layout view for the OAI21x1 cell.

# OAI22

**Cell Description:**This is a standard 4 input OR AND INVERT (OAI) cell. This cells functionality is described by the following Boolean equation:

**Truth Table:**

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| **A** | **B** | **C** | **D** | **Y** |
| 0 | 0 | 0 | 0 | 1 |
| 0 | 0 | 0 | 1 | 1 |
| 0 | 0 | 1 | 0 | 1 |
| 0 | 0 | 1 | 1 | 1 |
| 0 | 1 | 0 | 0 | 1 |
| 0 | 1 | 0 | 1 | 0 |
| 0 | 1 | 1 | 0 | 0 |
| 0 | 1 | 1 | 1 | 0 |
| 1 | 0 | 0 | 0 | 1 |
| 1 | 0 | 0 | 1 | 0 |
| 1 | 0 | 1 | 0 | 0 |
| 1 | 0 | 1 | 1 | 0 |
| 1 | 1 | 0 | 0 | 1 |
| 1 | 1 | 0 | 1 | 0 |
| 1 | 1 | 1 | 0 | 0 |
| 1 | 1 | 1 | 1 | 0 |

**Behavioral Verilog:**

//Verilog HDL for "Lib6710\_06", "OAI22X1" "behavioral"

module OAI22X1 ( Y, A, B, C, D );

input A;

input C;

output Y;

input D;

input B;

assign Y = ~((A | B) & (C | D));

specify

(A => Y) = (1.0, 1.0);

(B => Y) = (1.0, 1.0);

(C => Y) = (1.0, 1.0);

(D => Y) = (1.0, 1.0);

endspecify

endmodule

**Cell Size:**

|  |  |  |
| --- | --- | --- |
| **Drive Strength** | **Height (μM)** | **Width (μM)** |
| INVX1 | 27.0 | 12.0 |

**Performance:**

**Propagation Delay (Rising Outputs):**

|  |  |  |
| --- | --- | --- |
| **Drive Strength** | **Min.** | **Max.** |
|  |  |  |

**Propagation Delay (Falling Outputs):**

|  |  |  |
| --- | --- | --- |
| **Drive Strength** | **Min.** | **Max.** |
|  |  |  |

**Output Fall Time:**

|  |  |  |
| --- | --- | --- |
| **Drive Strength** | **Min.** | **Max.** |
|  |  |  |

**Output Rise Time:**

|  |  |  |
| --- | --- | --- |
| **Drive Strength** | **Min.** | **Max.** |
|  |  |  |

**Logic Symbol:**

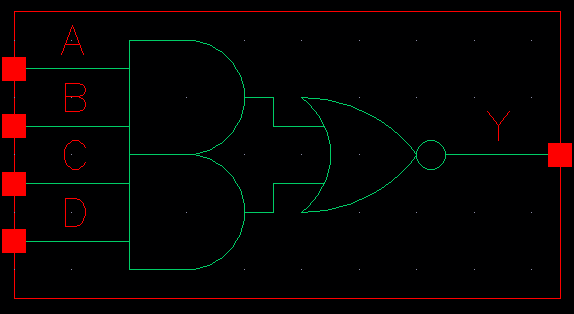
****

Figure 1: Symbol View for the OAI22 cell.

**CMOS Schematic:**

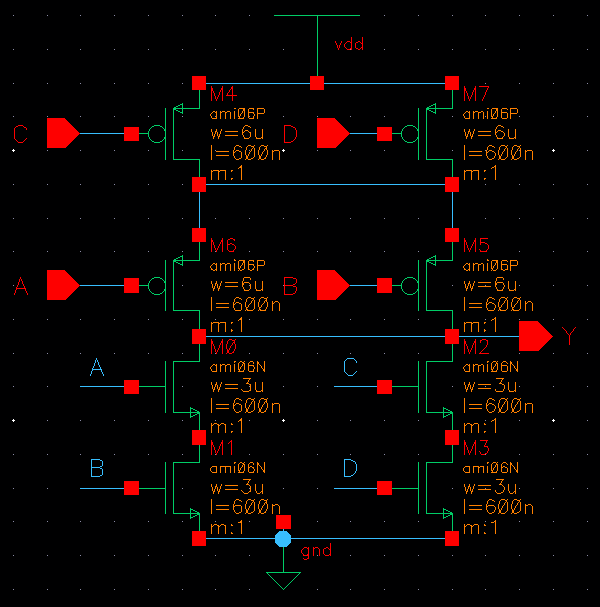
****

Figure 2: CMOS Schematic for the OAI22x1 cell.

**CMOS Layout:**

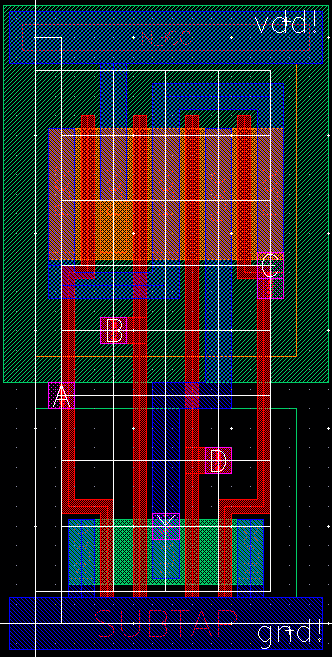
****

Figure 3: CMOS layout for the OAI22X1 cell.

# TIEHI

**Cell Description:**This is a standard TIEHI cell. The purpose of this cell is to hardcode a logic high signal. It is described by the following Boolean equation.

**Truth Table:**

|  |
| --- |
| **Y** |
| 1 |

**Behavioral Verilog:**

**Cell Size:**

|  |  |  |
| --- | --- | --- |
| **Drive Strength** | **Height (μM)** | **Width (μM)** |
| TIEHI | 27.0 | 4.8 |

**Logic Symbol:**

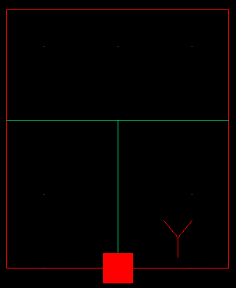
****

Figure 1: Symbol View for the TIEHI cell.

**CMOS Schematic:**

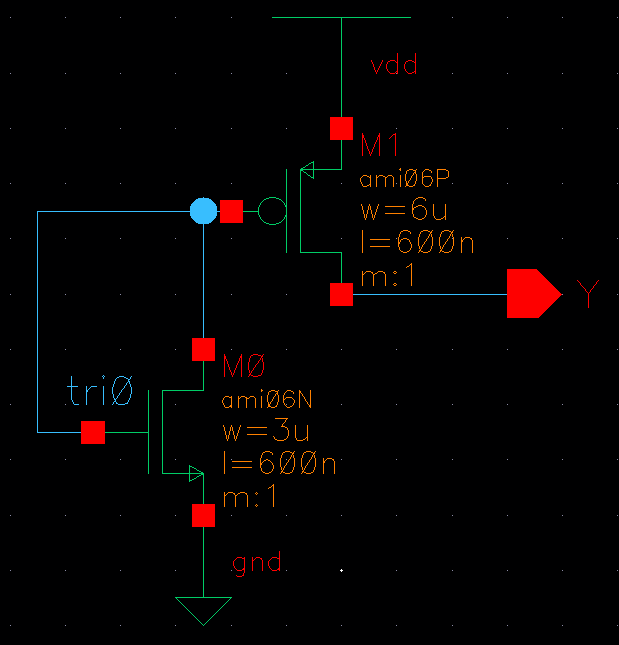
****

Figure 2: CMOS Schematic for the TIEHI cell.

**CMOS Layout:**

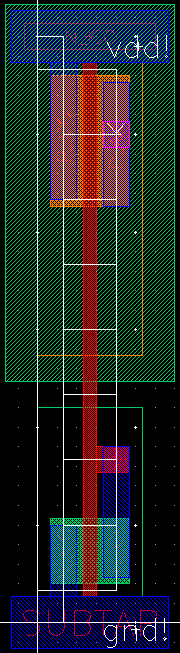
****

Figure 3: CMOS layout for the TIEHI cell

# TIELO

**Cell Description:**This is a standard TIELO cell. The purpose of this cell is to hardcode a logic low signal. It is described by the following Boolean equation.

**Truth Table:**

|  |
| --- |
| **Y** |
| 0 |

**Behavioral Verilog:**

//Verilog HDL for "Lib6710\_06", "TIELO" "behavioral"

module TIELO ( Y );

output Y;

assign Y = 1'b0;

endmodule

**Cell Size:**

|  |  |  |
| --- | --- | --- |
| **Drive Strength** | **Height (μM)** | **Width (μM)** |
| TIELO | 27.0 | 4.8 |

**Logic Symbol:**

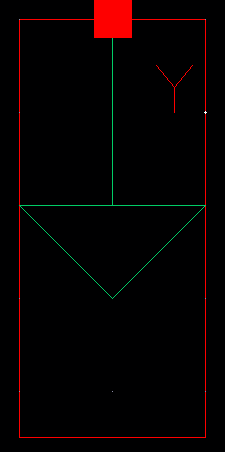
****

Figure 1: Symbol View for the TIELO cell.

**CMOS Schematic:**

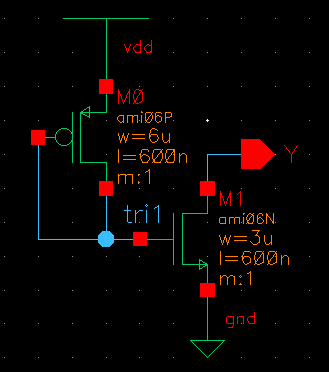
****

Figure 2:

**CMOS Layout:**

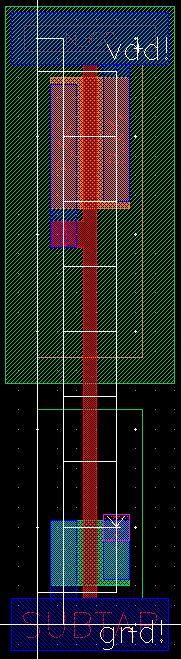
****

Figure 3: CMOS layout for the TIELO cell

# TRINV

**Cell Description:**This is a standard tristate inverter cell. This cells functionality is described by the following Boolean equation:

**Truth Table:**

|  |  |  |  |
| --- | --- | --- | --- |
| **A** | **P\_EN** | **N\_EN** | **Y** |
| 0 | 0 | 0 | 1 |
| 0 | 0 | 1 | 1 |
| 0 | 1 | 0 | Z |
| 0 | 1 | 1 | Z |
| 1 | 0 | 0 | Z |
| 1 | 0 | 1 | 0 |
| 1 | 1 | 0 | Z |
| 1 | 1 | 1 | 0 |

**Behavioral Verilog:**//Verilog HDL for "Lib6710\_06", "TRINV" "behavioral"

module TRINV ( Y, A, N\_EN, P\_EN );

input A;

input N\_EN;

output Y;

input P\_EN;

assign Y = (N\_EN & ~P\_EN) ? ~A : 1'bz;

specify

(A => Y) = (1.0, 1.0);

(N\_EN => Y) = (1.0, 1.0);

(P\_EN => Y) = (1.0, 1.0);

endspecify

endmodule

**Cell Size:**

|  |  |  |
| --- | --- | --- |
| **Drive Strength** | **Height (μM)** | **Width (μM)** |
| TRINV | 27.0 | 7.2 |

**Performance:**

**Propagation Delay (Rising Outputs):**

|  |  |  |
| --- | --- | --- |
| **Drive Strength** | **Min.** | **Max.** |
| TRINV |  |  |

**Propagation Delay (Falling Outputs):**

|  |  |  |
| --- | --- | --- |
| **Drive Strength** | **Min.** | **Max.** |
| TRINV |  |  |

**Output Fall Time:**

|  |  |  |
| --- | --- | --- |
| **Drive Strength** | **Min.** | **Max.** |
| TRINV |  |  |

**Output Rise Time:**

|  |  |  |
| --- | --- | --- |
| **Drive Strength** | **Min.** | **Max.** |
| TRINV |  |  |

**Logic Symbol:**

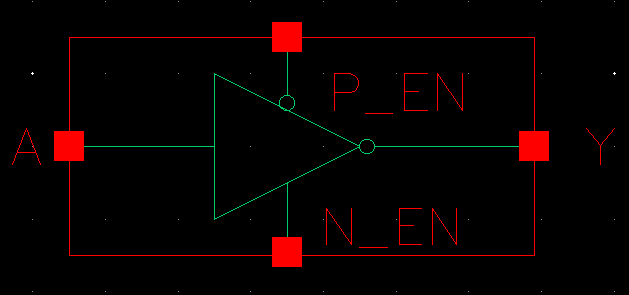
****

Figure 1: Symbol View for the TRINV cell

**CMOS Schematic:**

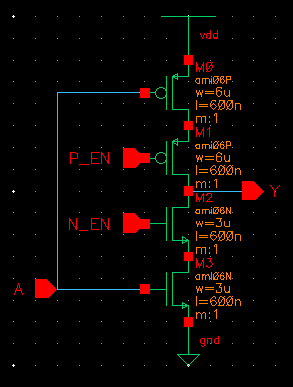
****

Figure 2: CMOS Schematic for TRINV cell.

**CMOS Layout:**

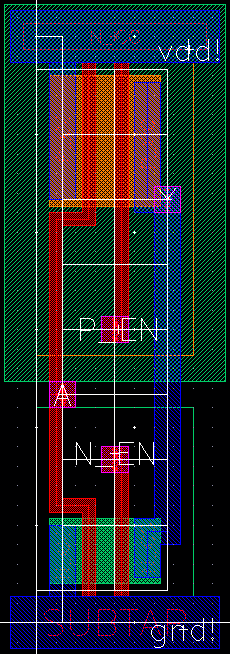
****

Figure 3: CMOS layout for TRINV cell.

# XOR

**Cell Description:**

This is a standard two input XOR cell with the following Boolean equation.

**Truth Table:**

|  |  |  |
| --- | --- | --- |
| **A** | **B** | **Y** |
| 0 | 0 | 0 |
| 0 | 1 | 1 |
| 1 | 0 | 1 |
| 1 | 1 | 0 |

**Behavioral Verilog:**

//Verilog HDL for "Lib6710\_06", "XOR2X1" "behavioral"

module XOR2X1 ( Y, A, B );

input A;

output Y;

input B;

xor(Y, A, B);

specify

(A => Y) = (1.0, 1.0);

(B => Y) = (1.0, 1.0);

endspecify

endmodule

**Cell Size:**

|  |  |  |
| --- | --- | --- |
| **Drive Strength** | **Height (μM)** | **Width (μM)** |
| XOR2X1 | 27.0 | 12.0 |

**Performance:**

**Propagation Delay (Rising Outputs):**

|  |  |  |
| --- | --- | --- |
| **Drive Strength** | **Min. (nS)** | **Max. (nS)** |
| XOR2X1 | 0.309335 | 0.536119 |

**Propagation Delay (Falling Outputs):**

|  |  |  |
| --- | --- | --- |
| **Drive Strength** | **Min. (nS)** | **Max. (nS)** |
| XOR2X1 | 0.337925 | 3.873978 |

**Output Rise Time:**

|  |  |  |
| --- | --- | --- |
| **Drive Strength** | **Min. (nS)** | **Max. (nS)** |
| XOR2X1 | 0.249189 | 3.189955 |

**Output Fall Time:**

|  |  |  |
| --- | --- | --- |
| **Drive Strength** | **Min. (nS)** | **Max. (nS)** |
| XOR2X1 | 0.214332 | 3.063275 |

**Logic Symbol:**

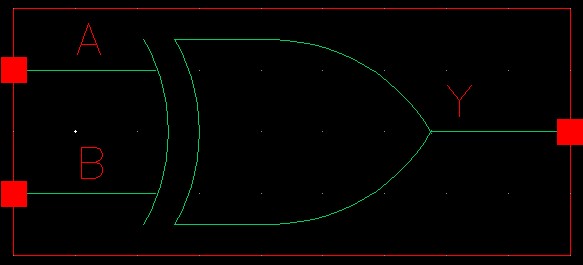
****

Figure 1: Symbol View for the XOR cell.

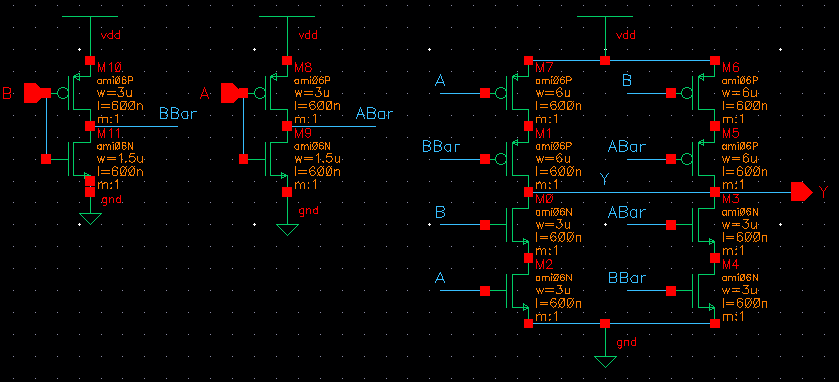
**CMOS Schematic:  
  
**

Figure 2: CMOS Schematic for the XOR2X1 cell.

**CMOS Layout:**

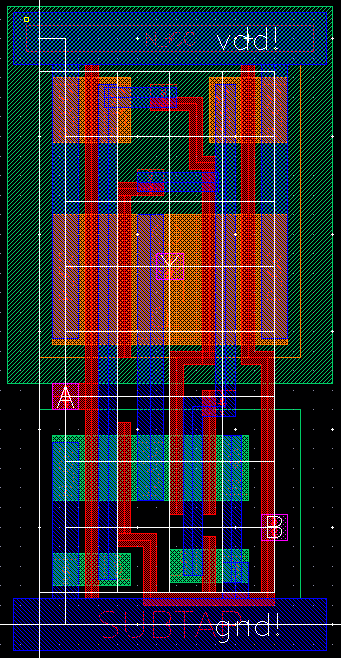
****

Figure 3: CMOS layout for the Nor2X1 cell.